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Electron beam direct writing technology combined with silicon shuttle service

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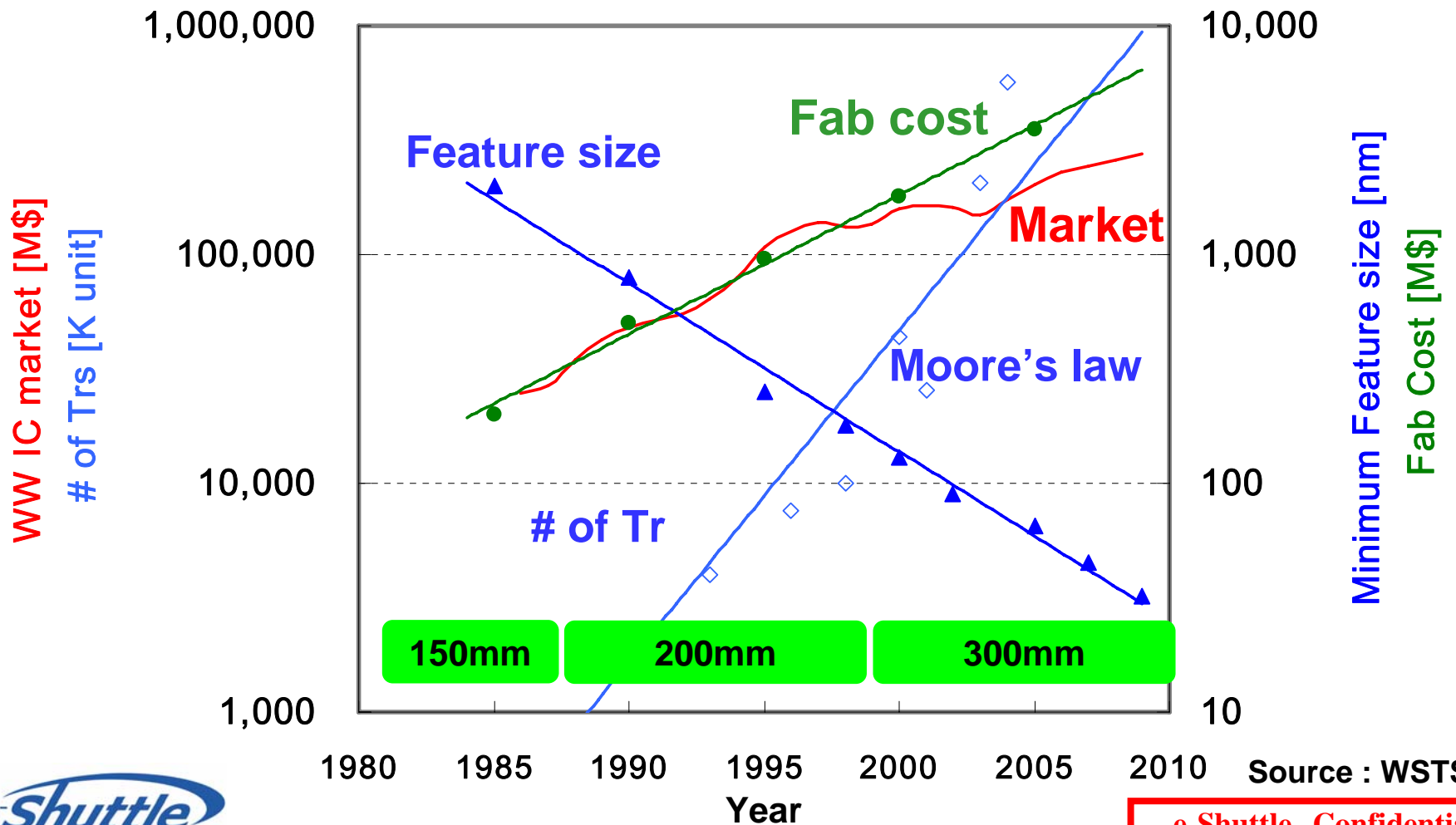
Today's talk outline

Discuss the economies of custom LSI prototyping, if EB lithography is implemented in the fab.

- **Review general trend and issues of custom LSI.**
- **Consider the availability of EB lithography for LSI prototyping.**
- **Propose optimized manufacturing scheme.**
- **Summary**

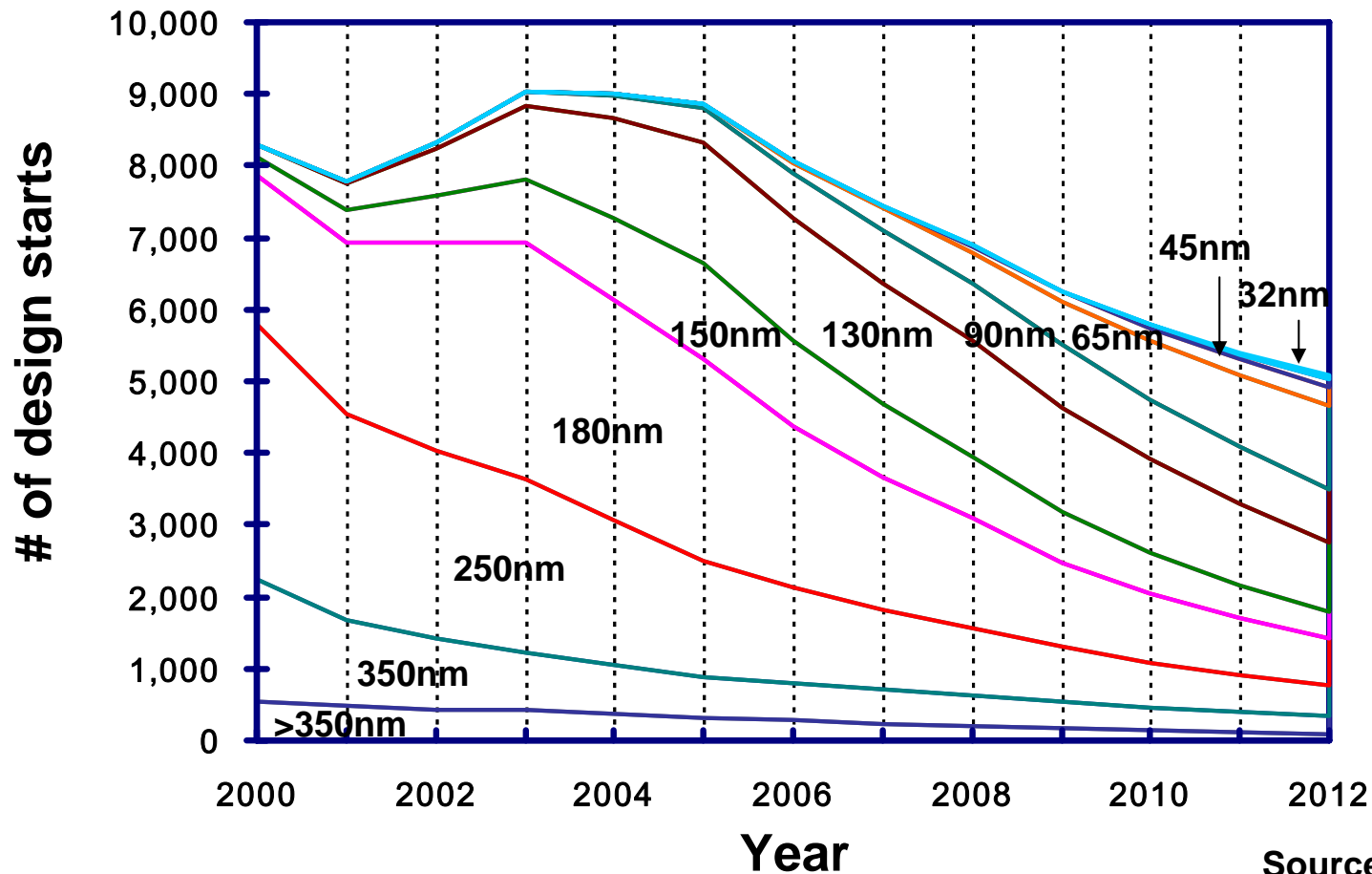
The semiconductor industry's history

Technology enables us to make Moore's law real, however the market growth rate has matured.



The custom LSI design starts trend

Semiconductor market has been continuously growing yet the number of design starts is declining year over year.



Source : IBS

A cost and design explosion in custom LSI

The entry barrier becomes high.
Missing the design opportunities

Year 2007

- Technology : 65nm
- # of gates : 100M
- Design cost : 2000

Year 2005

- Technology : 90nm
- # of gates : 10M
- Design cost : 1000

Year 2002

- Technology : 180nm
- # of gates : 2M
- Design cost : 100

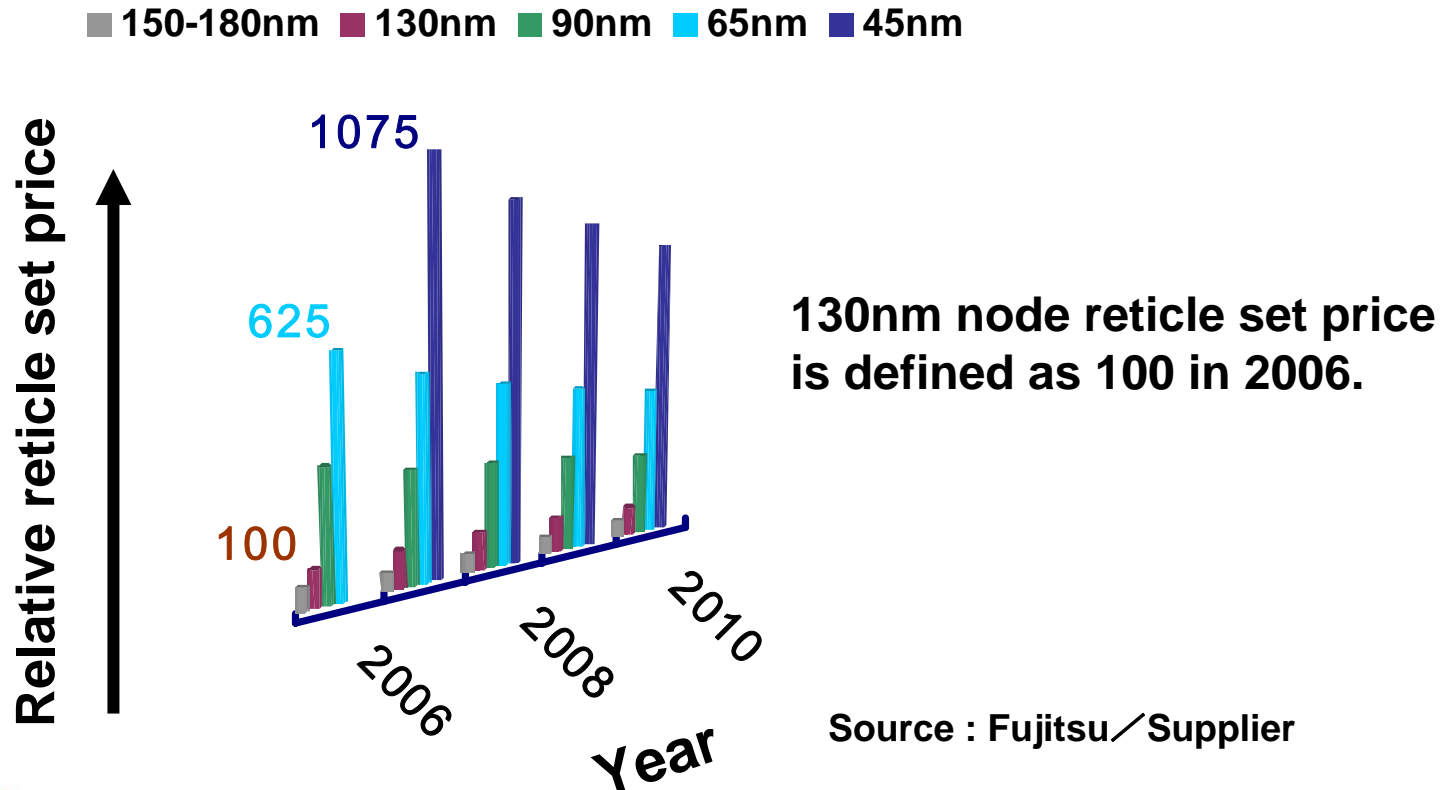
※ Cost is defined as 100 in the year 2002

Source : Fujitsu electronics Inc.

Pricing roadmap for cutting edge reticle

New generation reticle cost roadmap

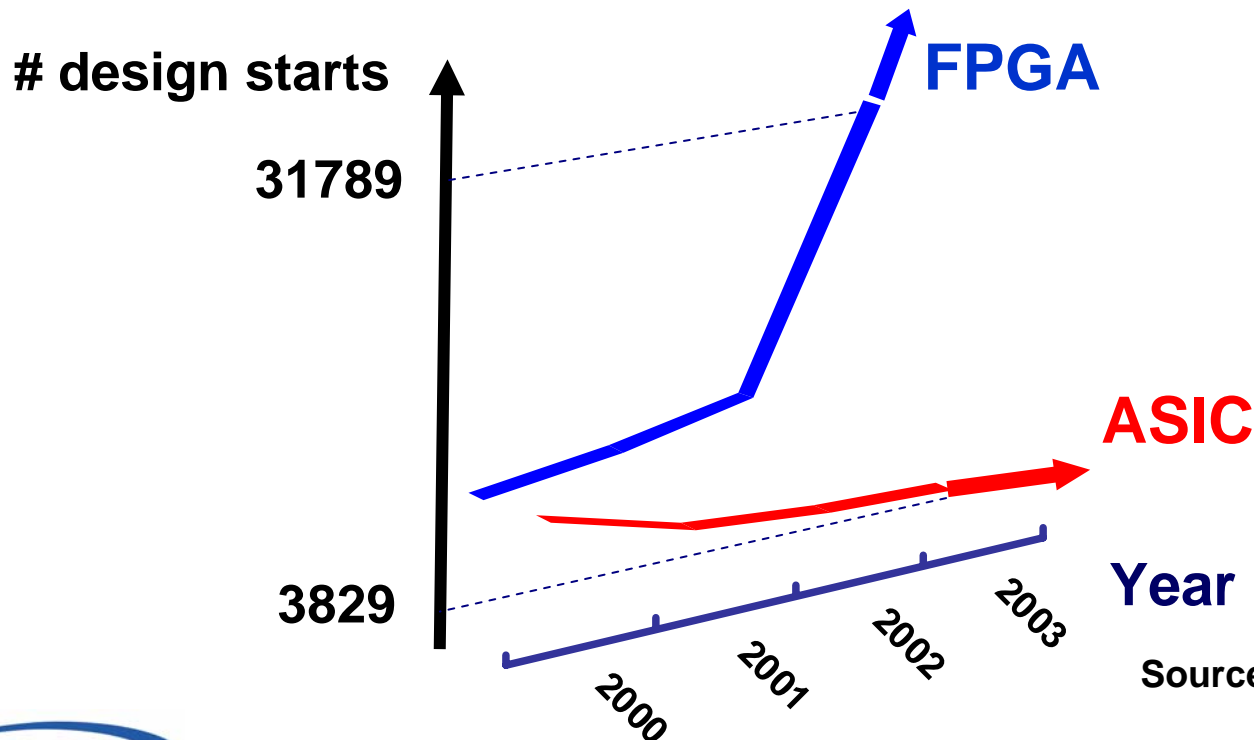
Reticle set price is going up. 65nm set is 6 times as high as 130nm set. 45nm is almost 10 times more.



Why are ASIC design opportunities being squeezed ?

The number of design starts

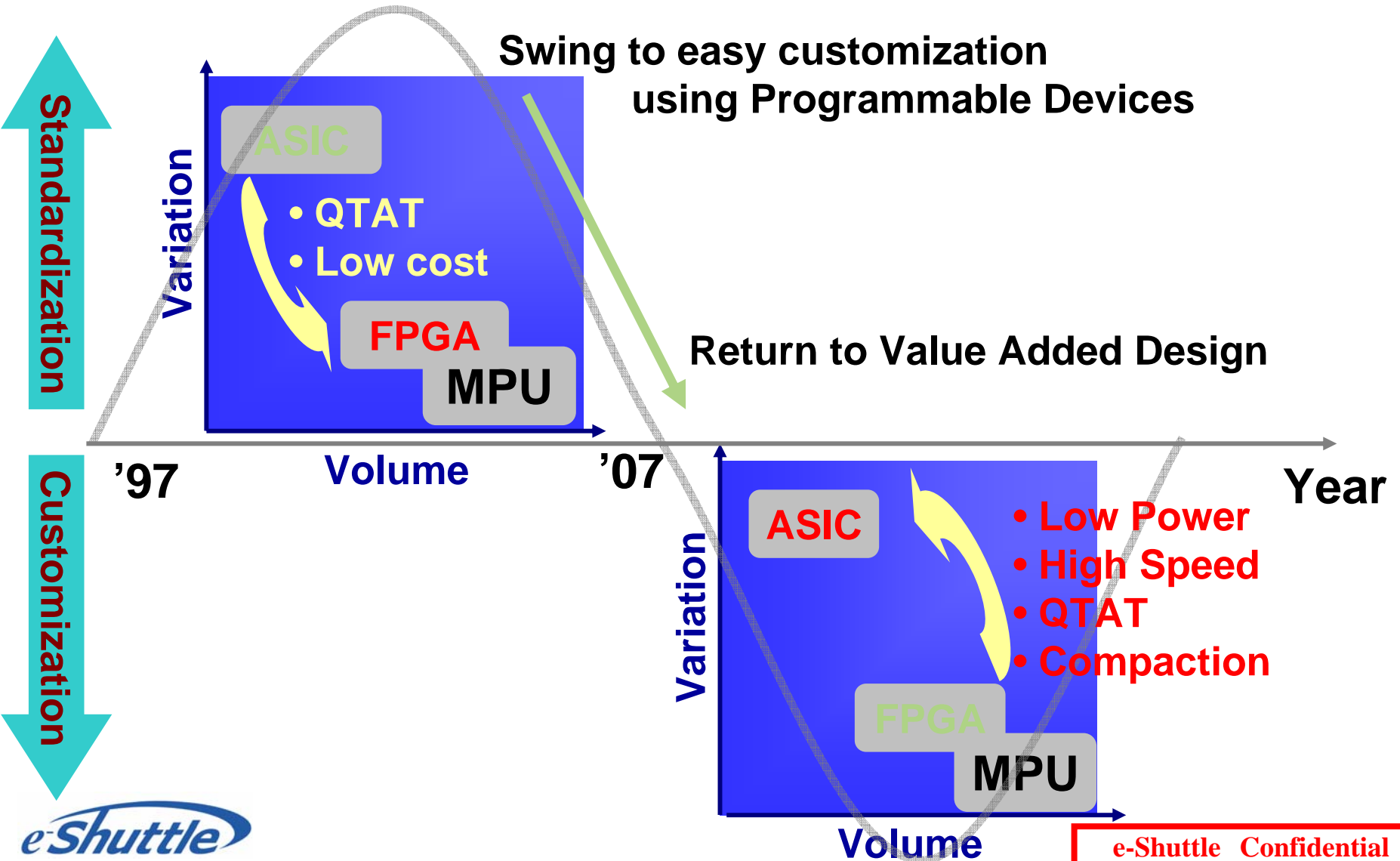
The number of design starts for FPGA has grown rapidly, but that for ASICs is declining. This is evidence that there are significant market opportunities for custom LSI design.



Source : Fujitsu/Supplier

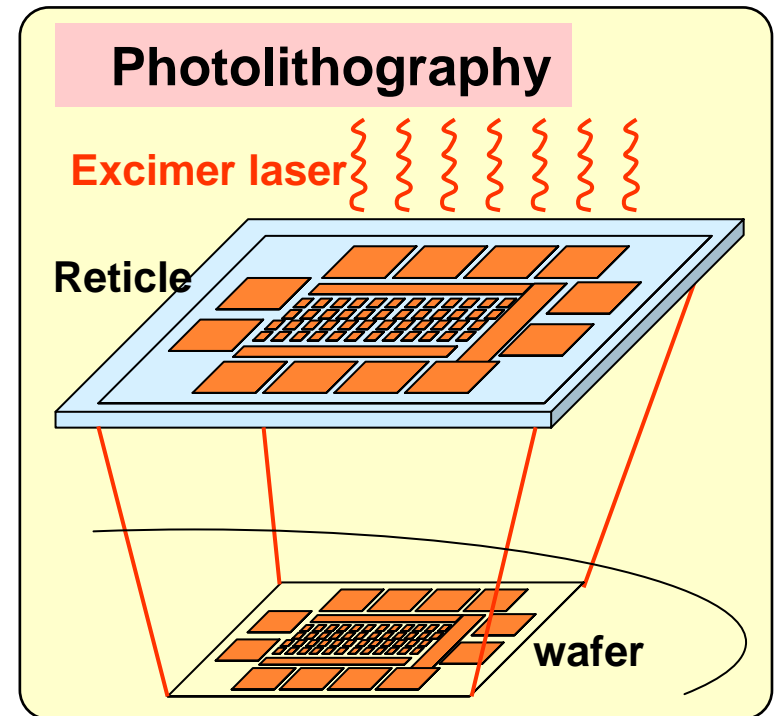
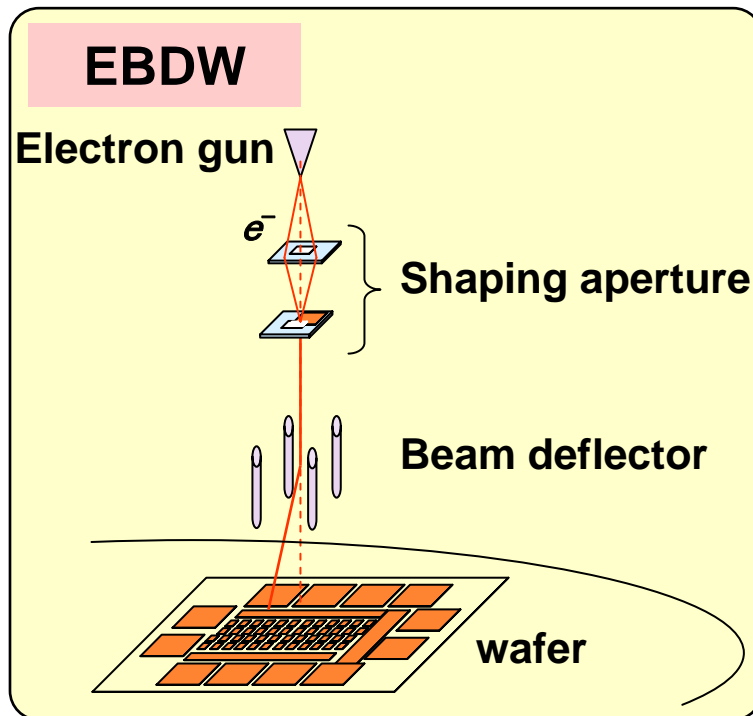
Makimoto's wave

Makimoto's wave swings from standardization to customization



EB Direct Writing (EBDW)

The Electron Beam Direct Writer transfers design data directly onto the resist coated wafer and exposes it.



■ Features

- No mask is necessary, pattern generation is direct and flexible.
- No complex data handling such as an optical pattern correction.

The cost restructuring by EB lithography

The most expensive part for 65nm reticle set is the fine interconnection layer.

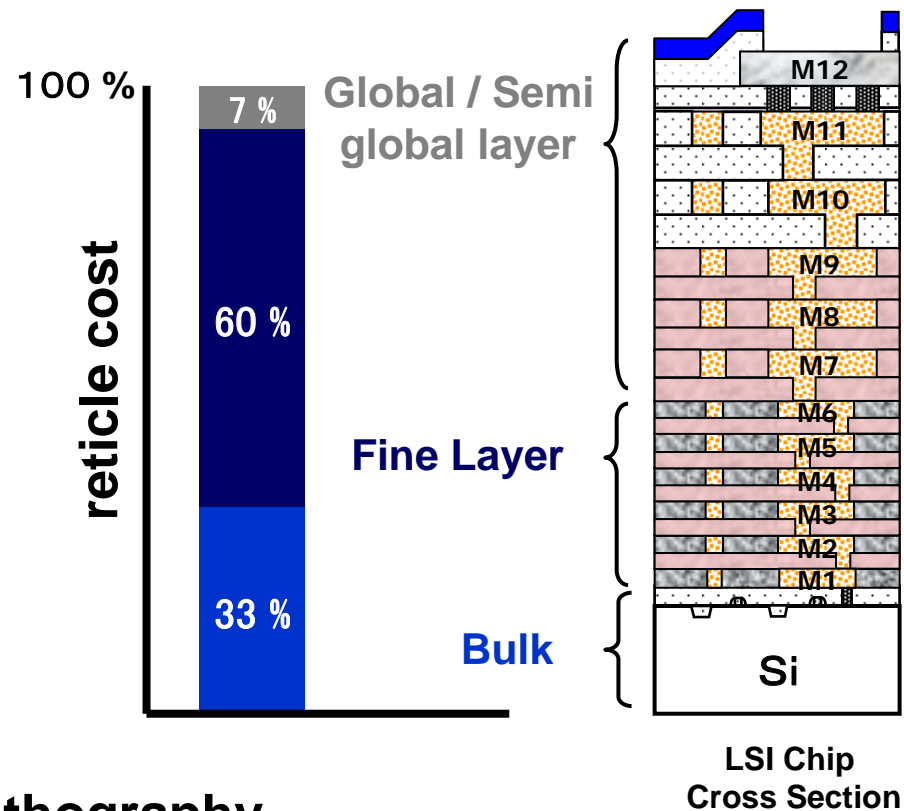
Scenario 1)

If all fine layers are replaced by EB lithography, 60% of reticle cost will be saved.

Scenario 2)

If FEOL reticle is replaced by EB lithography, total turn around time will be shortened.

65nm node reticle cost components



Source: Fujitsu

The advantage of prototyping using EB

EB tool is able to lower the barrier of re-spin opportunities

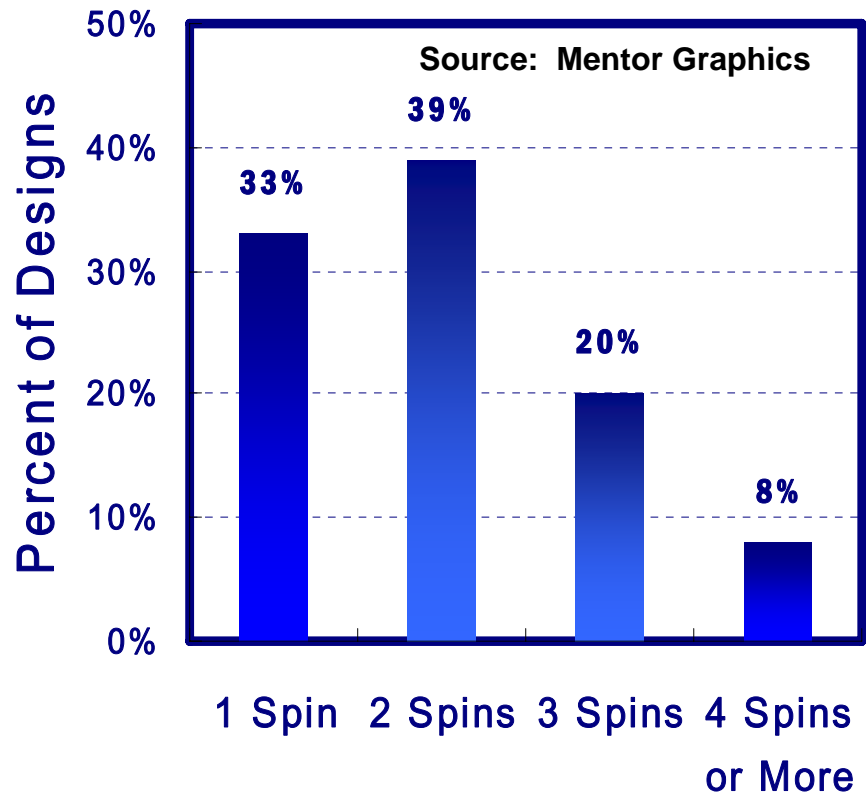
Issues

- ◆ A lot of re-spin requirements
- ◆ As a result, boost in verification tools cost.

Benefits

- ◆ Easy to adapt for re-spin needs.
- ◆ Easy to adapt for derivative design.
- ◆ Saving recovery time and opportunity cost.

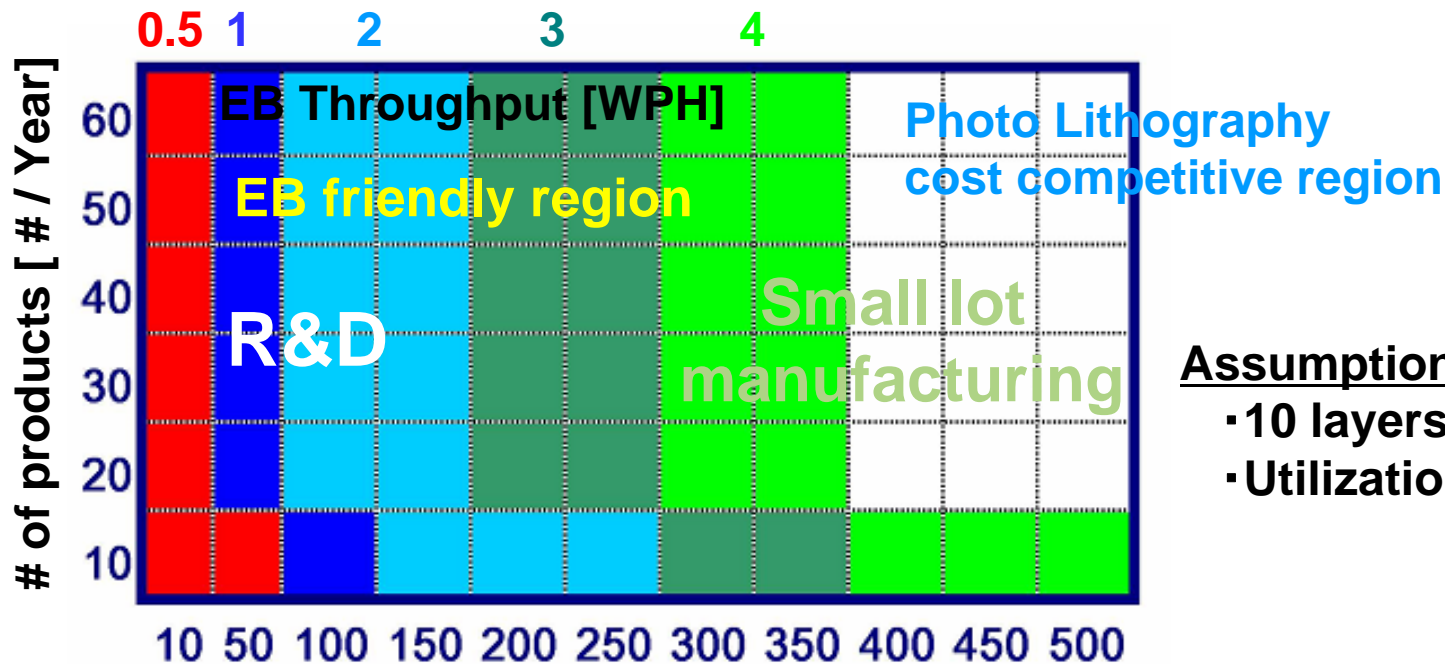
Si Spins required to release ASIC



Wafer production cost competitive plot

The higher EB throughput creates new production scheme.

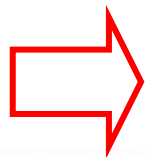
The cost competitive region map for EB lithography



Assumptions :

- 10 layers drawn with EB.
- Utilization of EB is 75%.

The total # of annual production wafers [# / products]



The improvement of EB throughput could extend to small lot manufacturing region

The shuttle services using EB direct writing

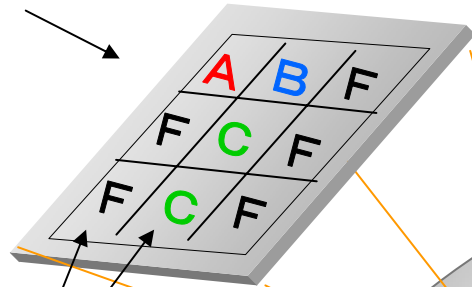
LSI prototyping by multi-project wafer

Shared reticle

(block by block)

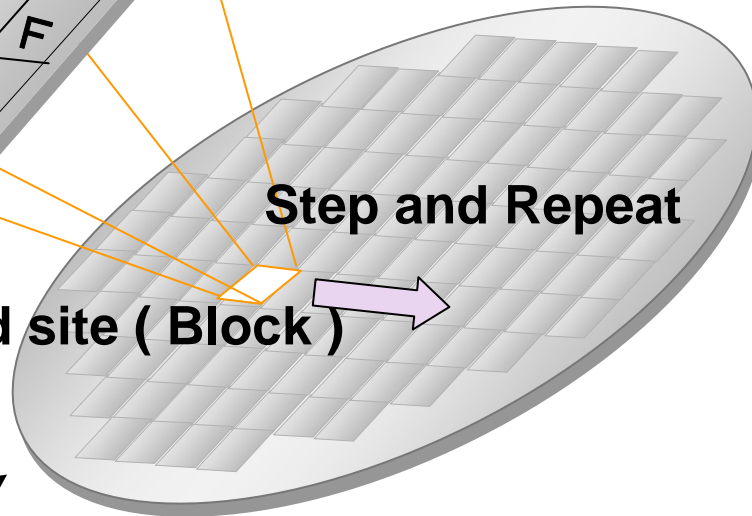


EB shuttle possibilities are



Customer owned site (Block)

Step and Repeat



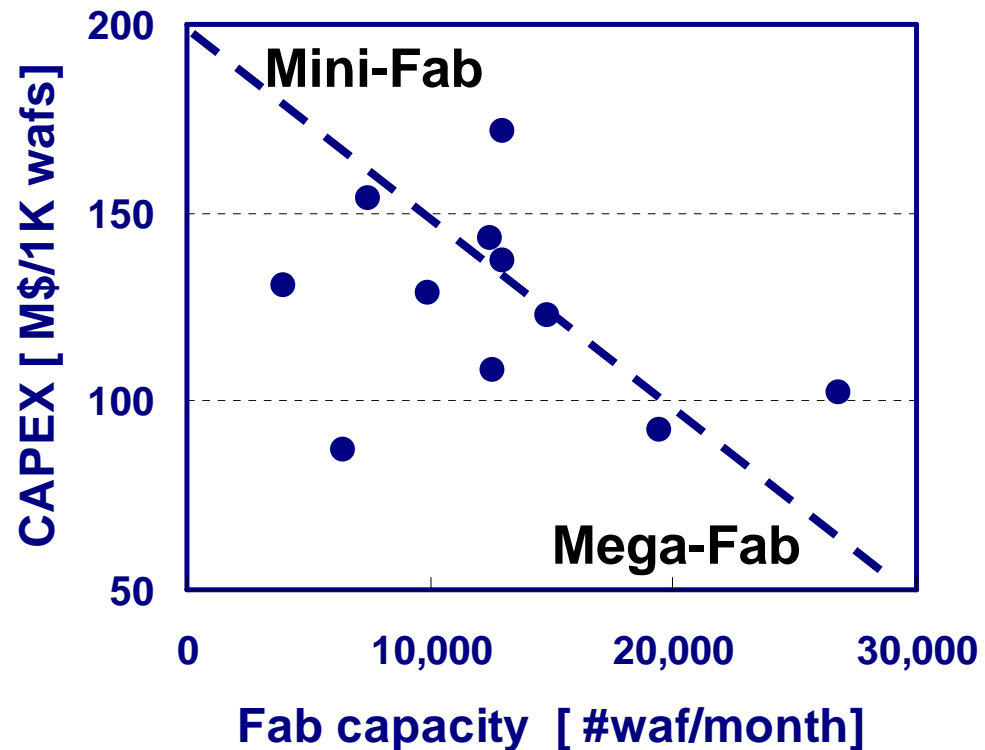
65nm process 300mm wafer

- ◆ Easy trimming
 - ▶ Site by site
- ◆ Easy respins
 - ▶ On demand
- ◆ Mask set cost
 - ▶ Savings

Significance of adding EB shop to mega-fab

The prototyping manufacturing efficiency may have improved to implement the EB shop on Mega-fab for following reasons.

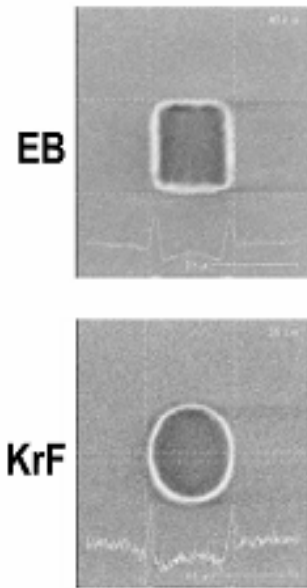
- A mega-fab is dedicated to volume production.
- A mini-fab is economically inefficient and poorly scalable.
- The EB shop implemented into mega-fab could fill these gaps.
- Photo-compatible EB technique is key to bridge between products and prototypes.



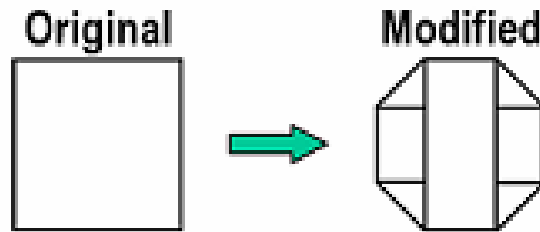
Source: SEC company filing 10K,20F

Pattern modification techniques

Drawing data modification to maintain photo-compatible patterning has been developed.



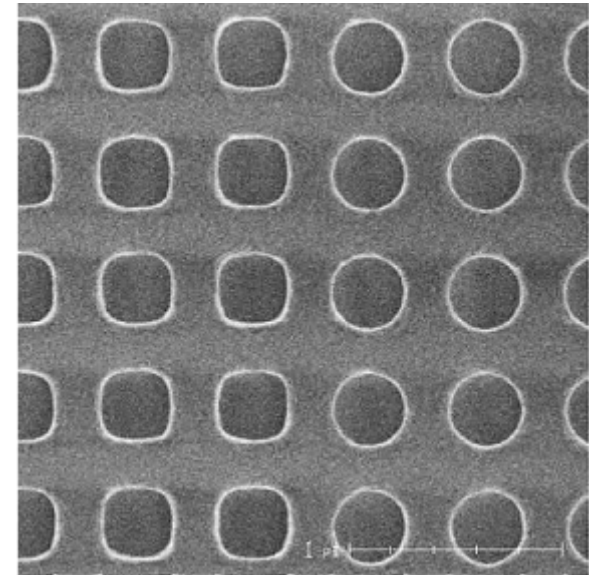
Octagonal reshaping



EB pattern

Original

Modified



Source: Fujitsu

A shape identical to the one from optical exposure can be obtained by using EB exposure.

The EB shop realizes overhead reduction

Reduced work load enables us to make use of EB lithography.

EB lithography

Photolithography

Saving material and opportunity cost

Lot in

2 weeks or more

Sign off

Lot in

1 day

Pattern Correction

DFM checker

Spend many resources:
e.g.

Data formatting

OPC verification

EDA tools.
A lot of time.
Human assets .

Sign off

Design completion (GDS out)

EB shop in volume production fab

300mm
Fab

300mm 1st line 15K waf / month (Full operation)

300mm 2nd line 25K waf / month (Installing now)

EB shop
e-Shuttle Inc.

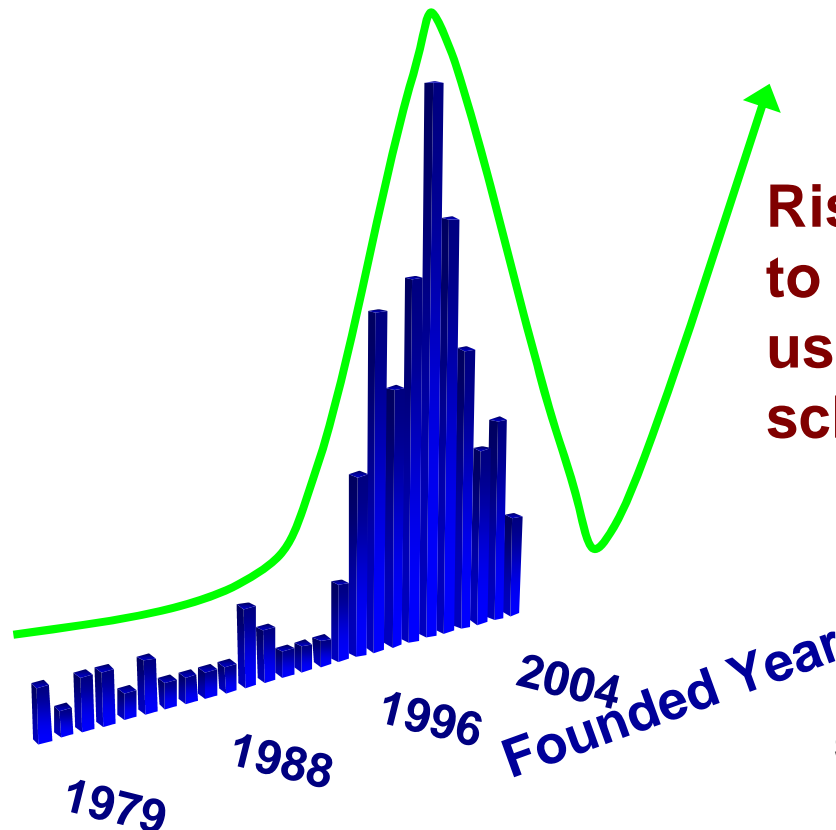


Advantest EBDW F3000

Fujitsu's Mie plant

Lowering prototyping barrier opens a new frontier

Cost pressure for first silicon might reduce the number of newcomers. Our scheme would remove the entry barrier, and provides opportunities for accelerated R&D to newcomers.



Rising up to the challenge to achieve a breakthrough using the new prototyping scheme.

Source: Venture Access

Summary

- The number of design starts has been decreasing year over year. Turnaround time and chip making cost have to be lowered to enhance custom LSI prototyping activities.
- An EB lithography is better than photolithography for small lot manufacturing from the financial viewpoint.
- Based on the photo-compatible EB technique, the EB shop added to a mega-fab could restructure the productivity of small lot manufacturing.
- We hope that our proposed scheme using EB will contribute to growth of custom LSI designers and ultimately will lead to new activity in the industry.

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