# EBDW technology for EB shuttle at 65nm node and beyond

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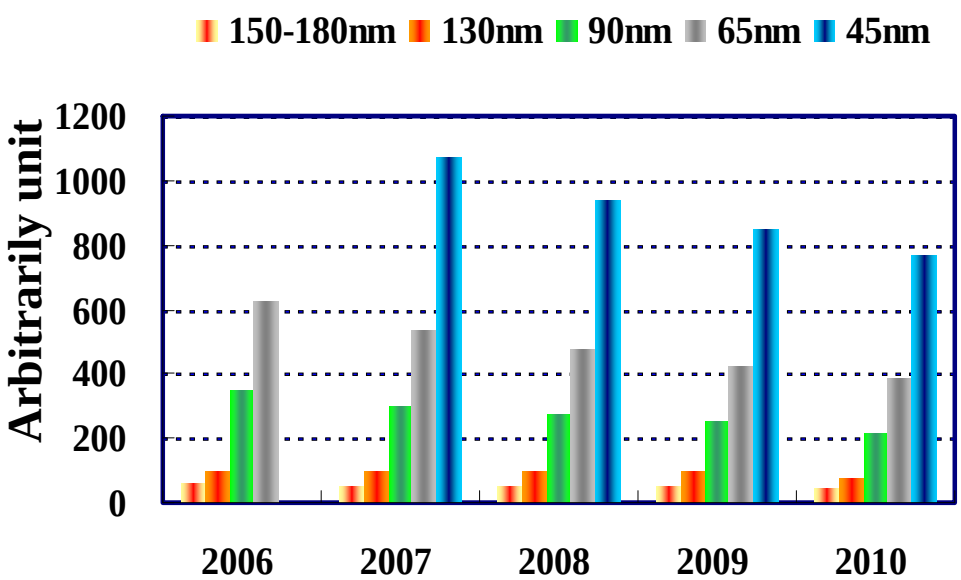
**(OUTLINE)**

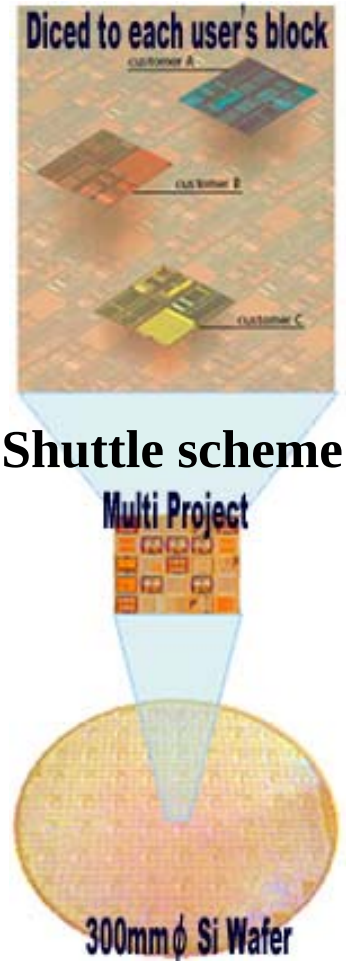
- **Background**
- **Exposure system**
- **Throughput**
- **CD control**
- **Proximity effect**
- **Resist process**
- **Critical issue at 45nm node**
- **SUMMARY**

# Reticle price rising and cost saving with EB shuttle scheme




**Reticle set price transition**
**130nm reticle set price in 2006=100**

Small groups difficult to get in touch leading edge technology




**Shuttle scheme**

e-Shuttle
300mm EB writer
F3000

**Fujitsu Mie plant**

- **Shuttle scheme (multi project) enables cost sharing**
- **EB Lithography enables less cost prototyping**

# Critical issues at 65nm EB shuttle process

⇒**PARTIAL BLOCK**

Throughput
Target ～0.5wafer@Hr

Resist
Collapse

**EB Shuttle**

CD control
Instability of VSB

⇒**Top Shape Control**

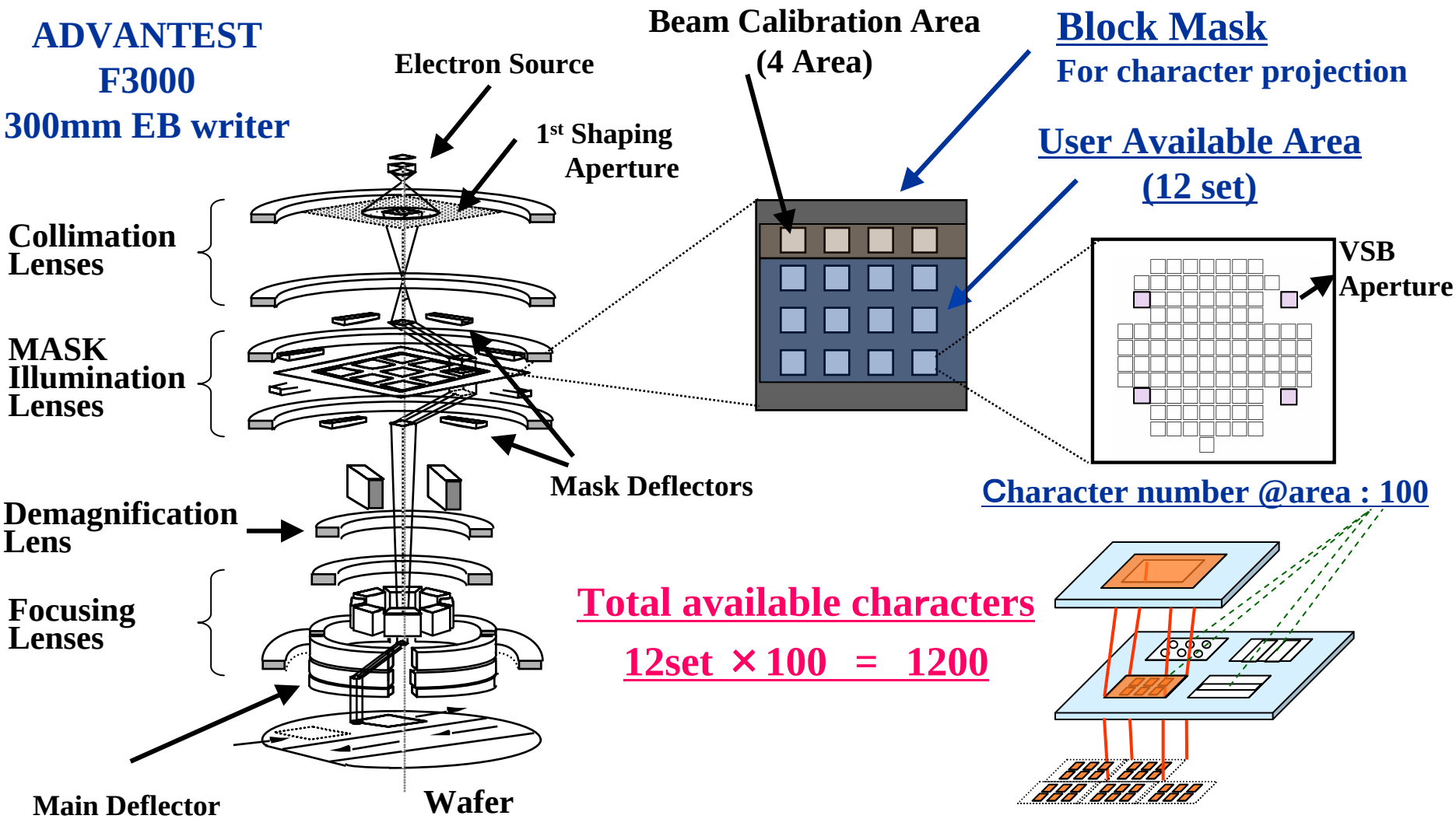
⇒**MASTER BLOCK**

3D Proximity effect at 50kV
Max 12 underlying layers

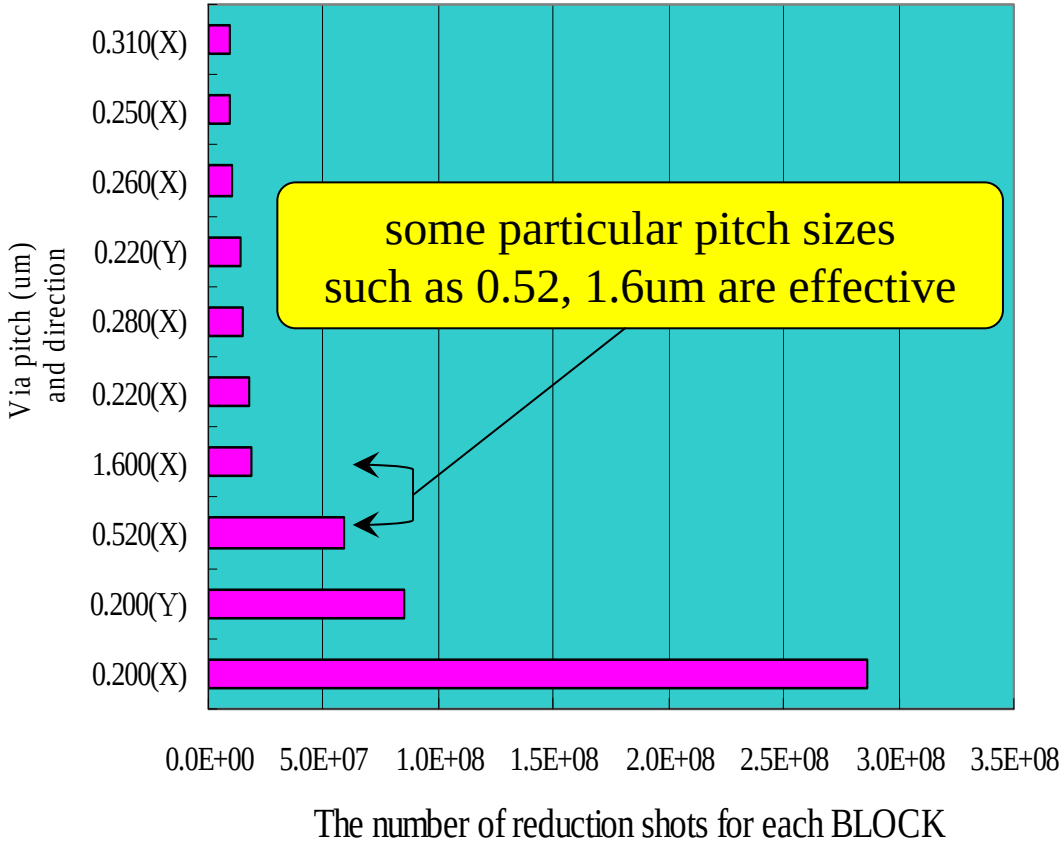
⇒**PC Cluster**

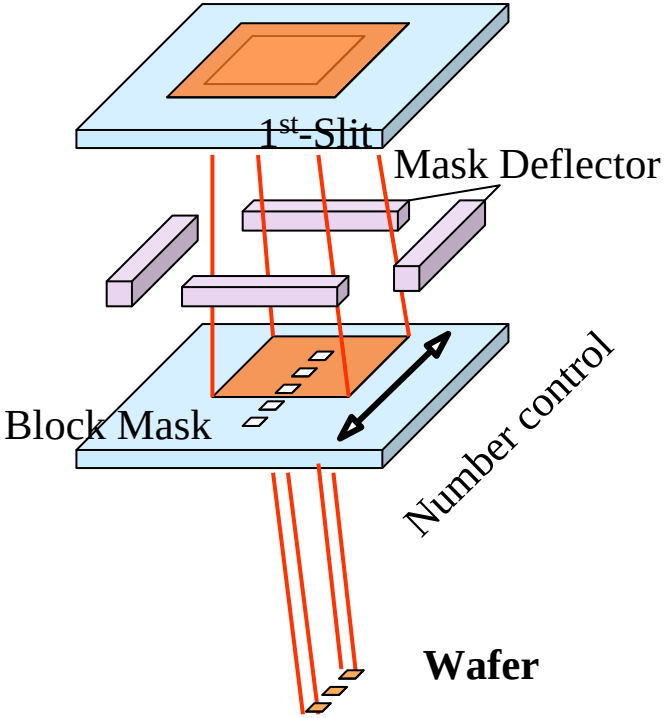
# BLOCK EXPOSURE system(F3000)

**ADVANTEST**
**F3000**
**300mm EB writer**



# Shot count reduction for via with PARTIAL BLOCK



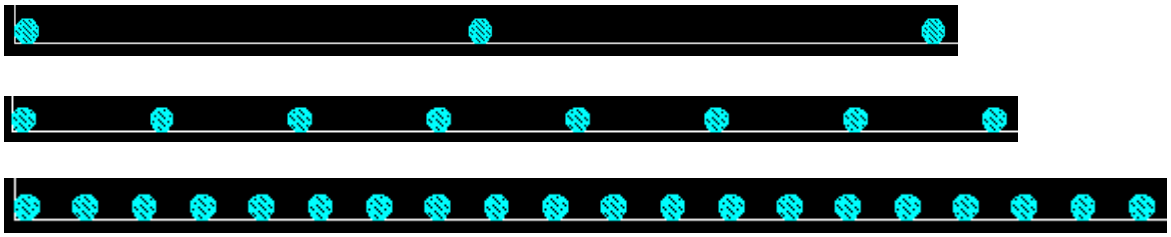




PARTIAL BLOCK Exposure

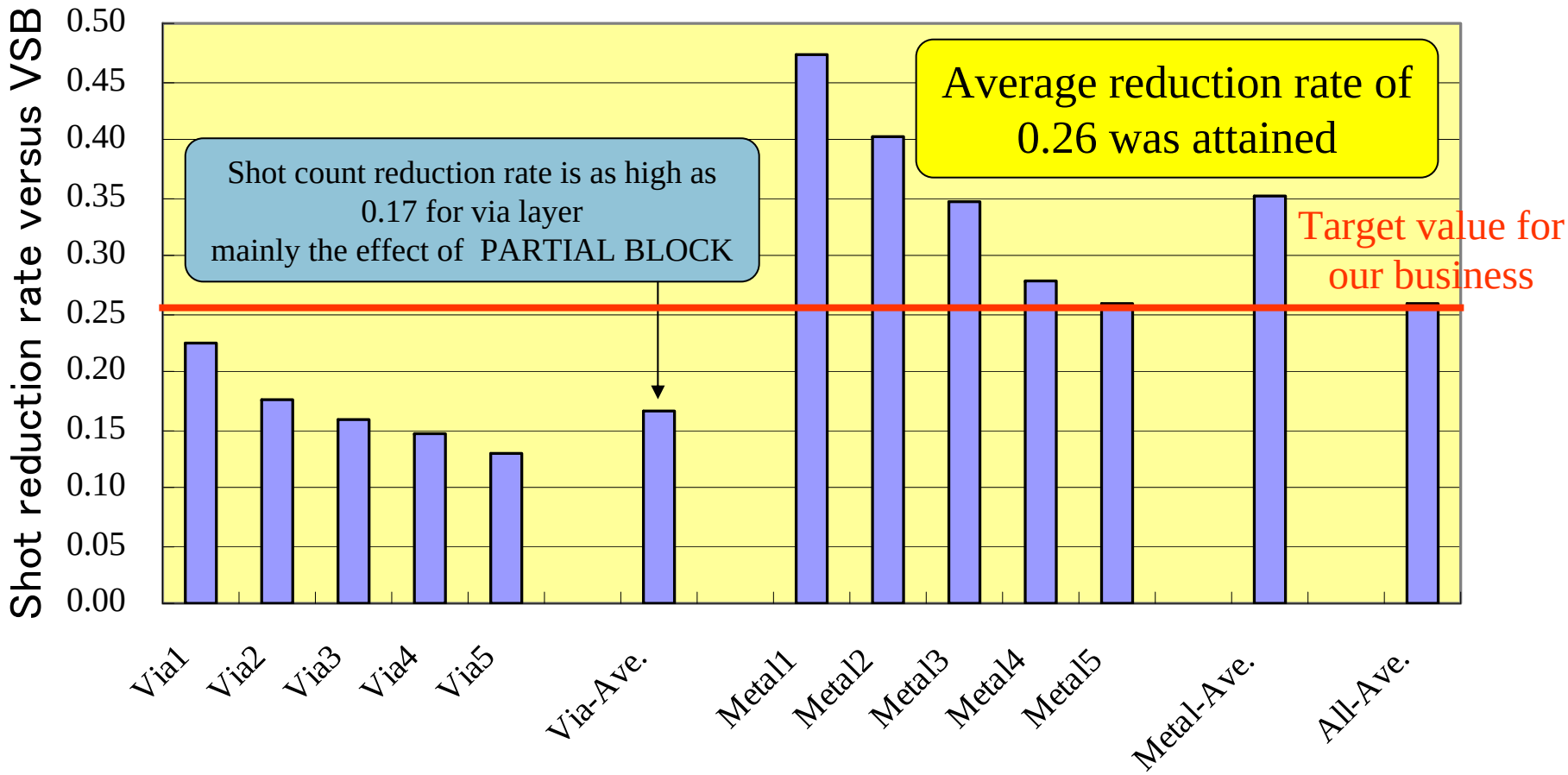
Pitch:1.6um

Pitch:0.52um

Pitch:0.2um



# Total shot count reduction with BLOCK EXPOSURE




- Average exposure shot count reduction rate of 0.26 was attained with applying BLOCK EXPOSURE to repeated via, CMP dummy, SRAM, ROM and so on

# Throughput improvement

**The scope of baseline capacity**
**300 layers/month**

⇨

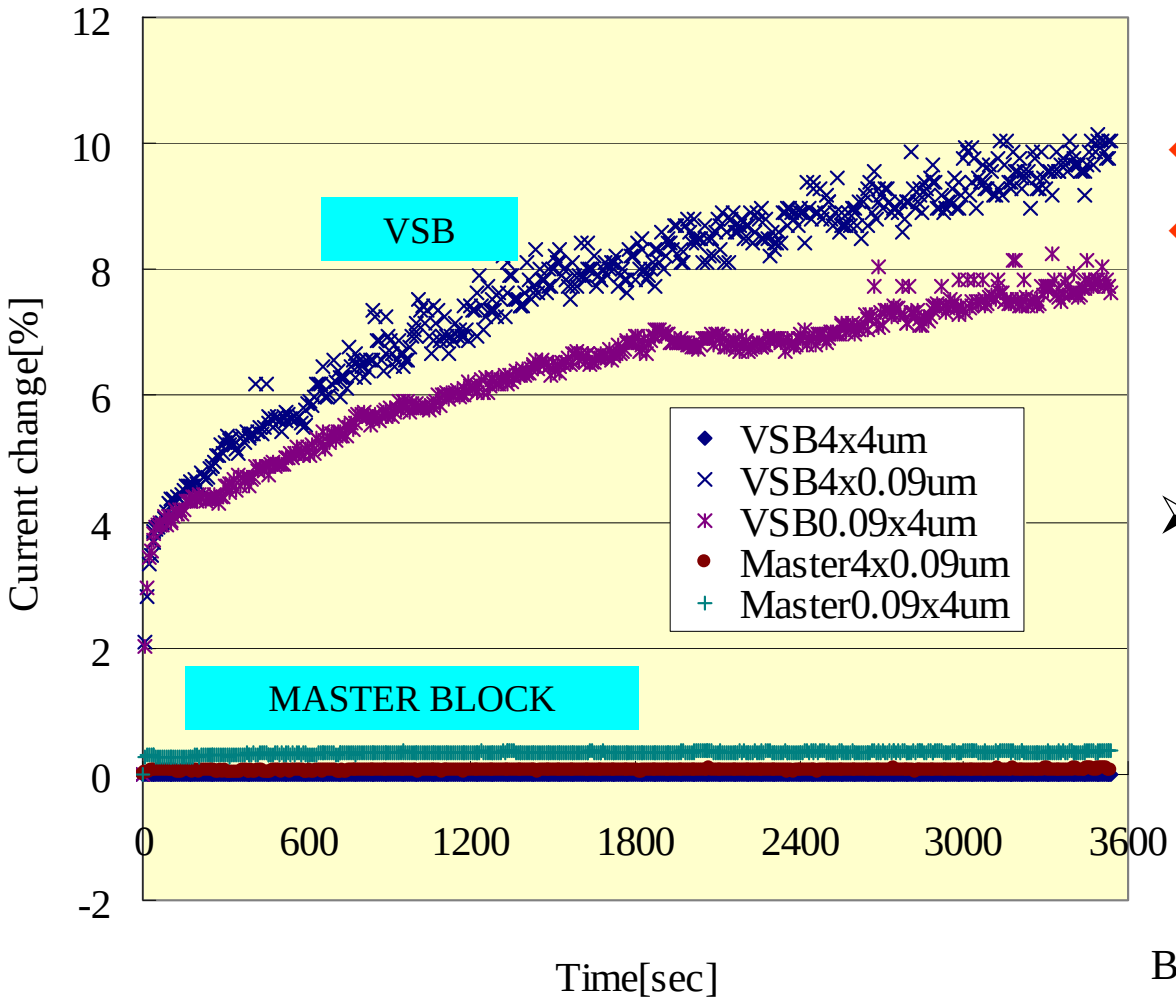
**Throughput requirement**
**baseline > 0.5WPH**

**The content of throughput restructuring**

| | Contribution Factor | # shot count dependent: Beam exposure | # shot count dependent: Settling | Shot count independent |
|---|---|---|---|---|
| VSB | 0.2WPH | 50% | 19% | 31% |
| | | Reduction rate ×0.26 | Reduction rate ×0.26 | ×0.77 |
| BLOCK EXPOSURE | 0.5WPH | 13% | 5% | 22% |
| | | Shot count reduction | | Improvement of drawing strategy (EB writer) |

➢ **Target throughput was attained mainly because using BLOCK EXPOSURE**

# Stability of beam current with MASER BLOCK



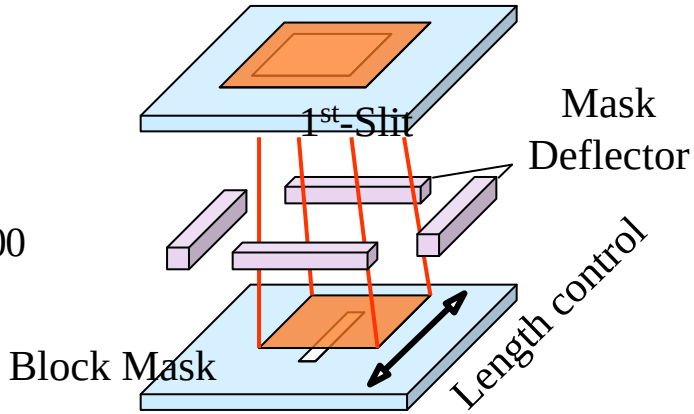

(VSB)

**Shows instability caused by**

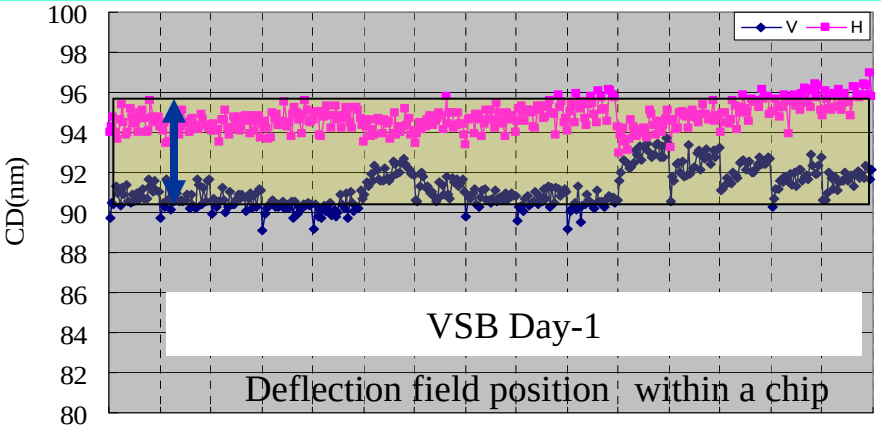
- **Mask position drift by heating**
- **Charging of deflector**

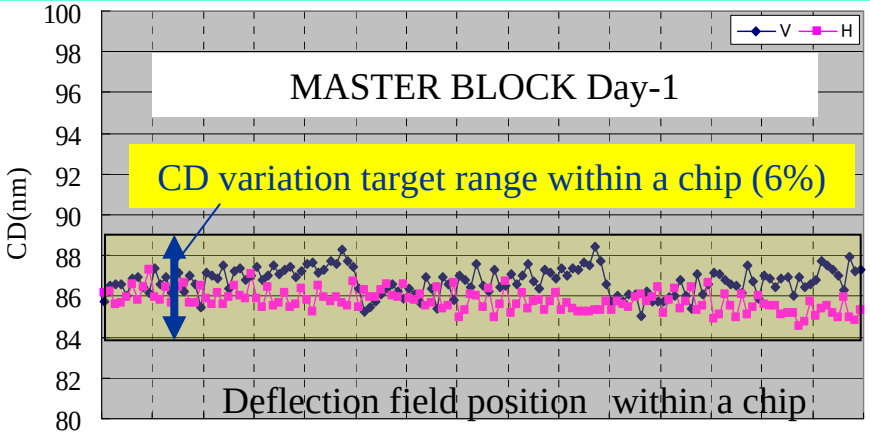
(MASTER BLOCK)

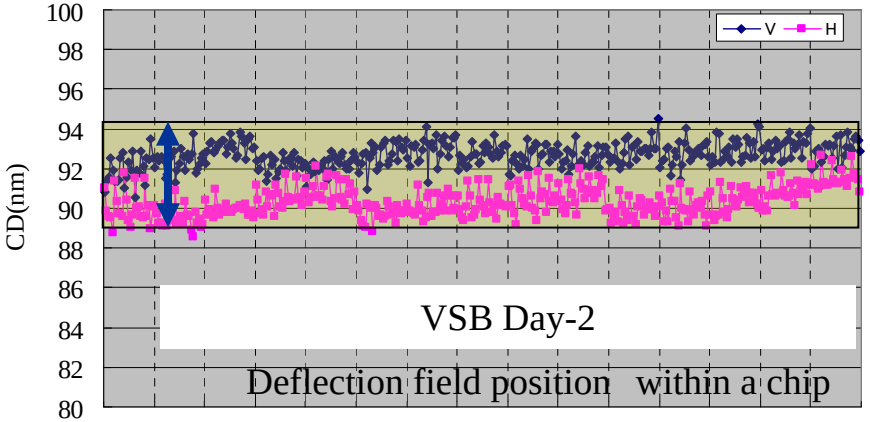
- **Good beam current stability**

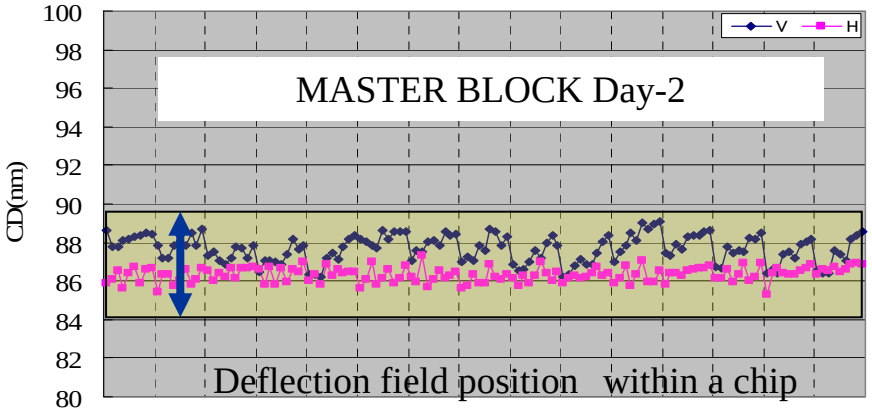


# CD stability data of MASTER BLOCK



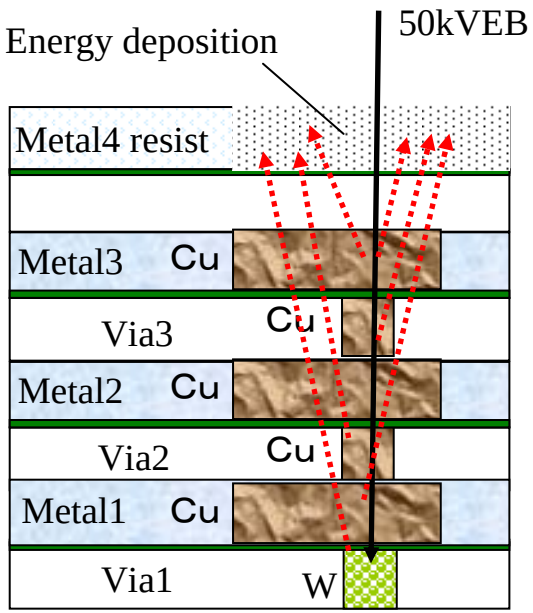



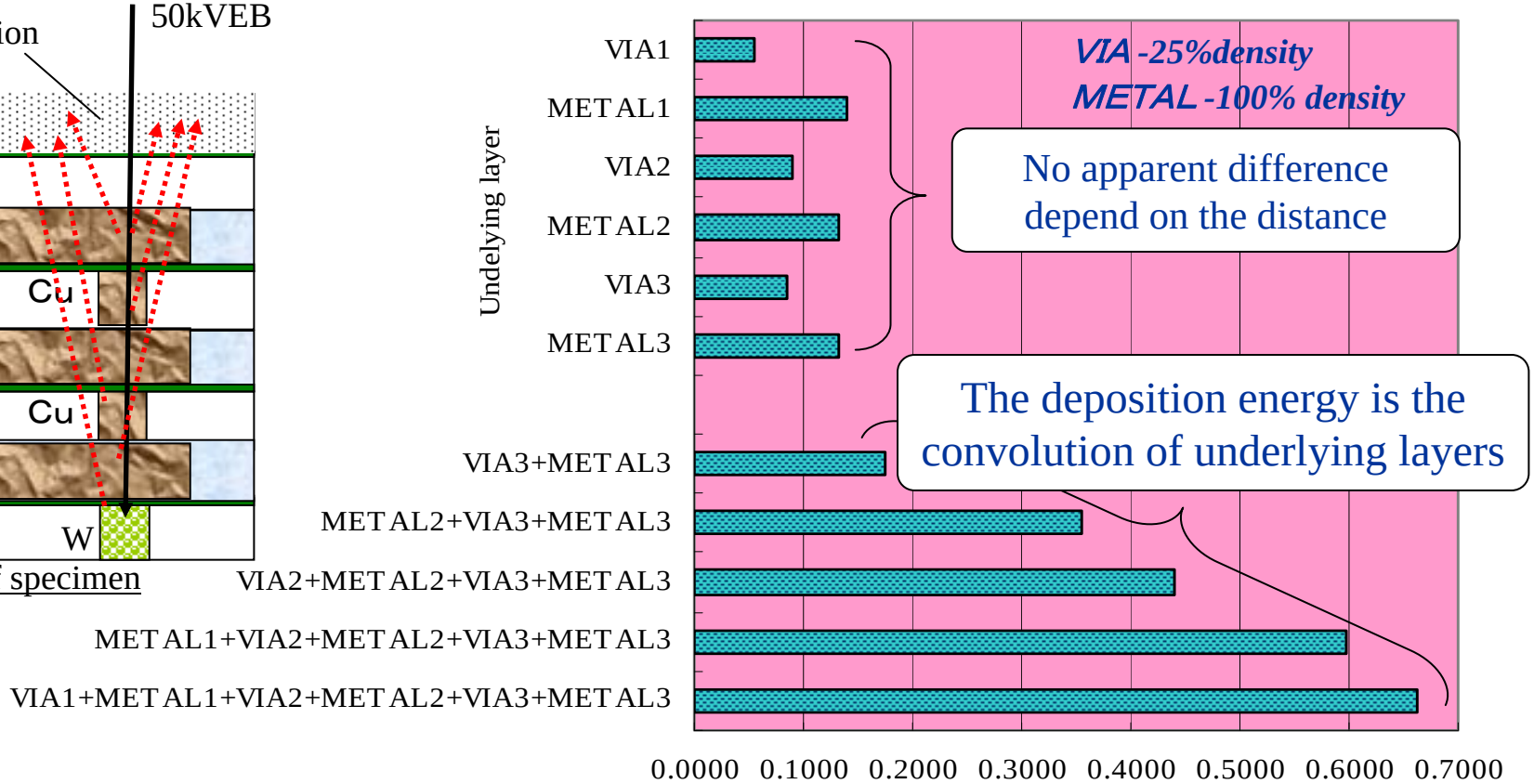

( MASTER BLOCK)

- Meets our CD variation target range within a chip (6%)
- Necessary for the 65nm devise manufacturing

# 3D multilayer proximity effect correction



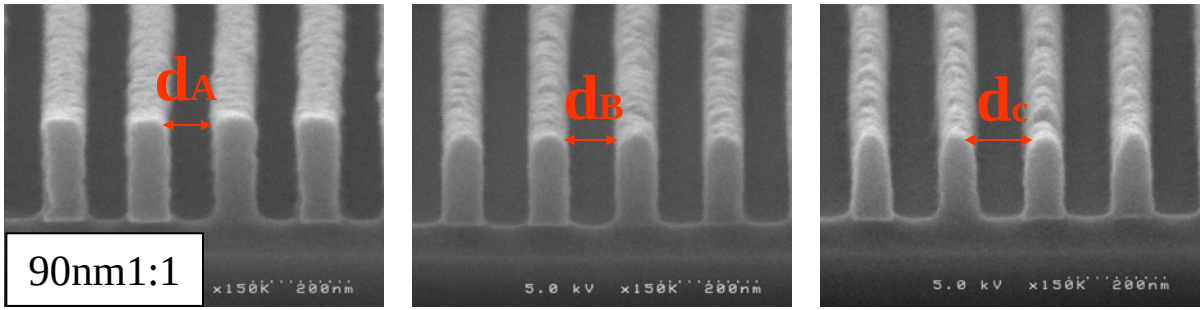

Structure of specimen




Amount of deposition energy by backscattering electron (au)

- All underlying heavy metal containing layers should be taken into account
- We enabled to calculate and correct multilayer proximity effect from max 12 underlying layers (for Metal7) with PC cluster

# Resist collapse control




**Resist pattern peeling force by the surface tension of the rinse liquid**

**: $F_x \propto 1/d_x$**

**Top width is dominant**

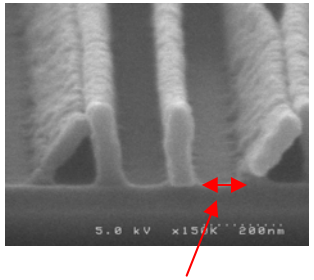
**$d_A < d_B < d_C$**

**⇒**

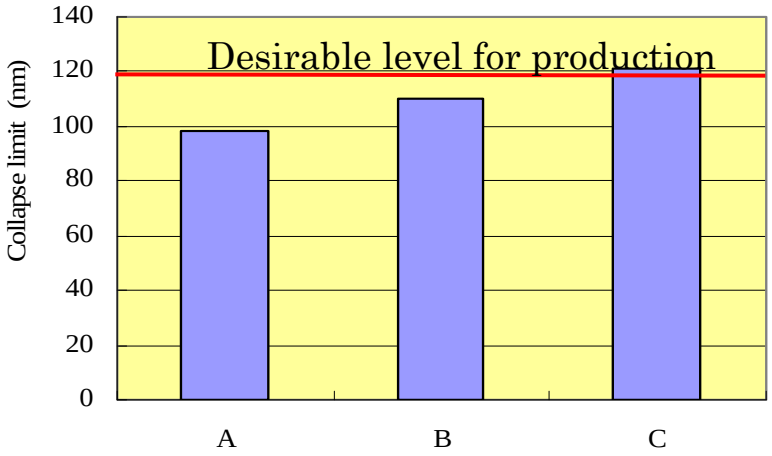
**$F_A > F_B > F_C$**

**Desirable shape for suppressing collapse**

**Customized by the tuning of base polymer, PAG, quencher**



Collapse limit CD (nm)

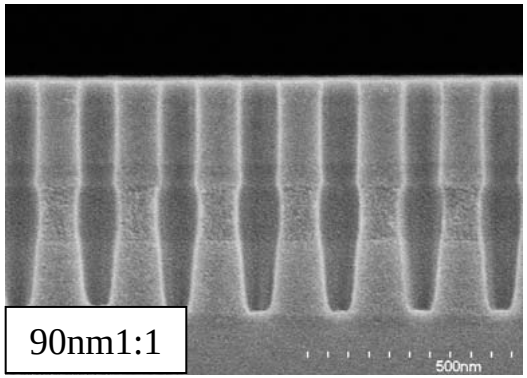



➢Top shape control enabled us to get enough durability for resist collapse

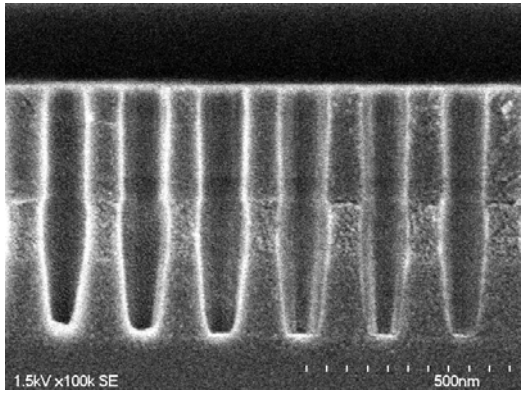
# Performed devise structures with EB lithography (65nm-node)

Cross sectional images of via patterns

**EB**

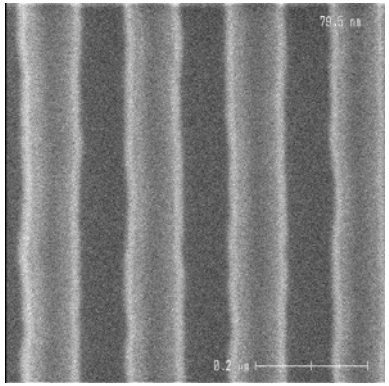



**ArF**

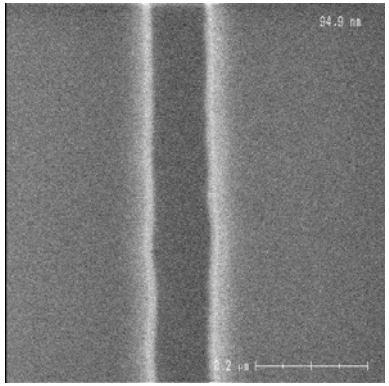



After etching

SEM images of metal interconnect patterns

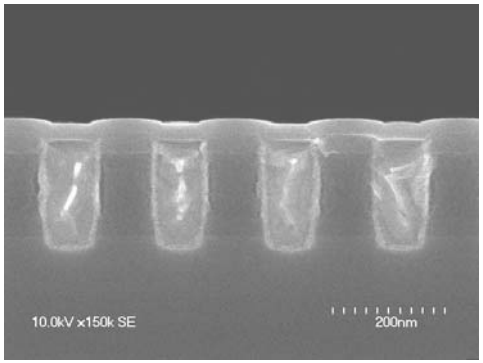


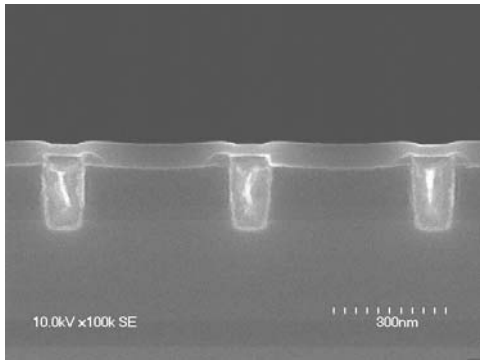
**0.1umLS**



**0.1um sparse**

After etching

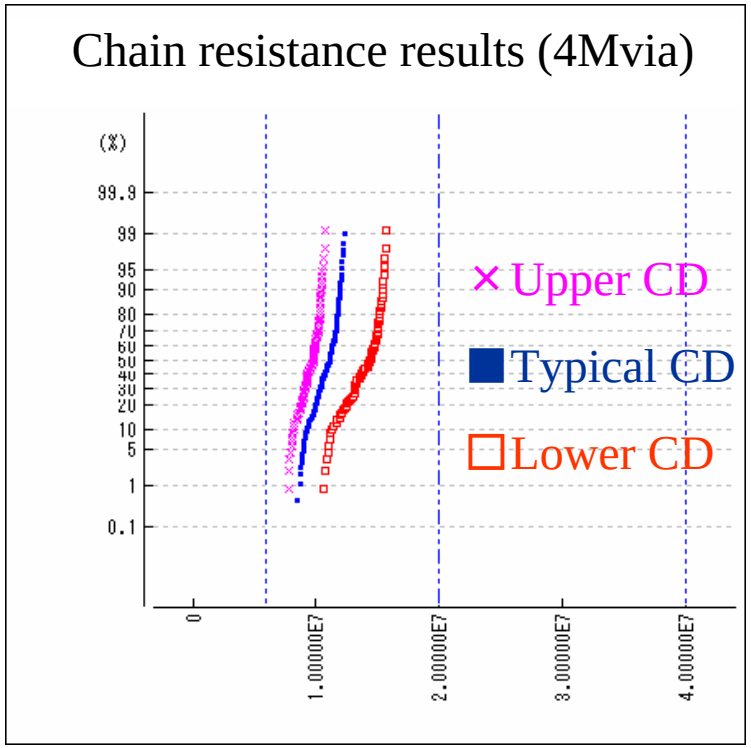


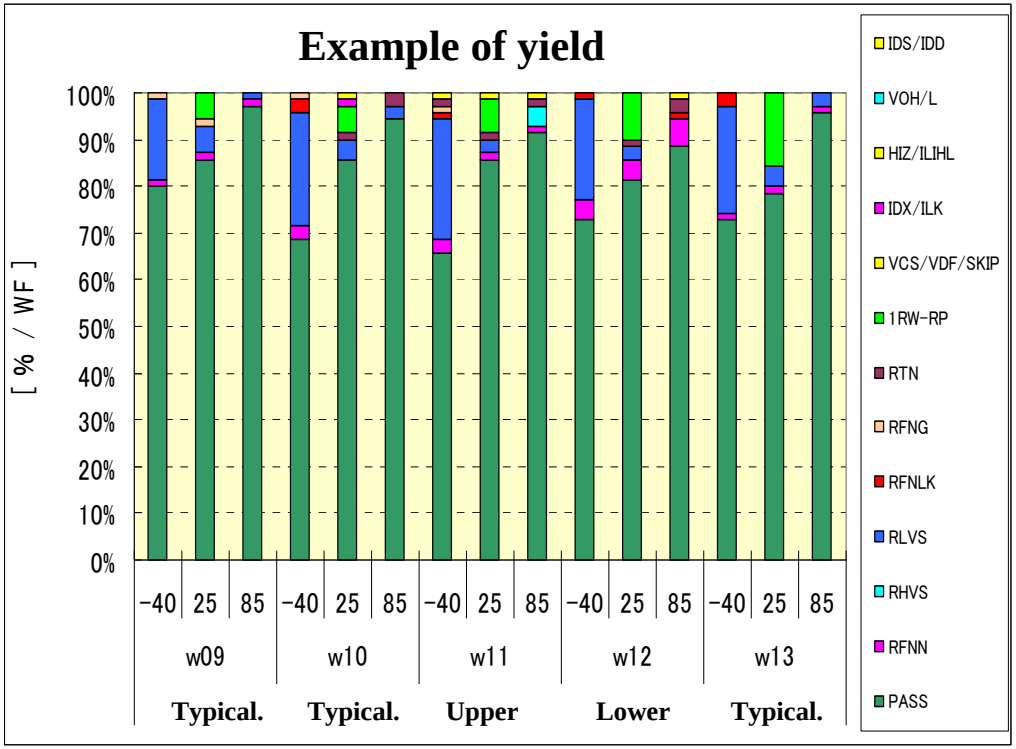




**After Cu CMP**

- Via shape of EBDW after etching has no particular difference with ArF
- 65nm node basic device structures were performed with EB lithography

# Electrical measurement results and yield in 65nm node



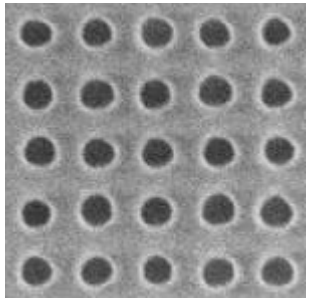




- Good electrical measurement results within CD control limit
- Enough yield for our target device was attained

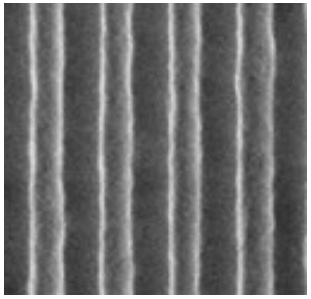
**⇒We have finished the verification of applying EB lithography to production.**

# Resist sensitivity issue at 45nm node

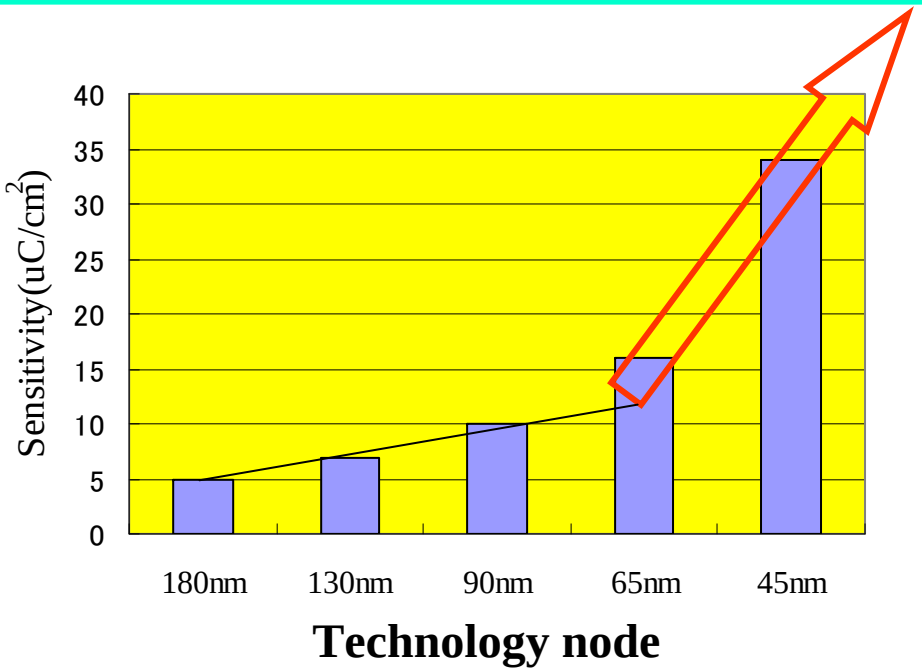
**45nm node**



**65nm 1:1 Via**
**29uC/cm2**



**60nmLS**
**38uC/cm$^2$**




◆**Resist sensitivity fall is skyrocketing and most critical issue at 45nm node**

- ✓**Shot count reduction with the DFM for EB**
- ✓**Increase of current density in EB writer**
- ✓**Resist material design feedback from EUV**

**Help me !**

# SUMMARY

- Throughput Target ～0.5wafer / Hr

⇒Shot count reduction rate of 0.26 with BLOCK EXPOSURE

- CD stability of fine size

⇒Precise CD control with MASTER BLOCK

- 3D proximity effect

⇒Enabled correction of all underlying layers with PC cluster

- Resist collapse

⇒Enough margin with top shape control

- 45nm node

⇒Resist sensitivity fall is most critical issue

**We have started 65nm EB shuttle business**

# Thank you very much.